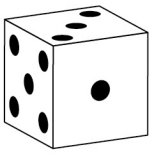
0 1 A die, where dots on the faces of a cube indicate the numbers 1 to 6, is shown in **Figure 3** and is used in many games.

Figure 3



A student makes an electronic version of this by feeding pulses from a pulse generator into a 4-bit binary counter.

The circuit uses the first three outputs of the counter A (least significant bit), B and C.

By feeding the outputs from the counter through logic gates, the seven LEDs shown in **Figure 4** can be made to display the numbers 1 to 6 in sequence.

Figure 4

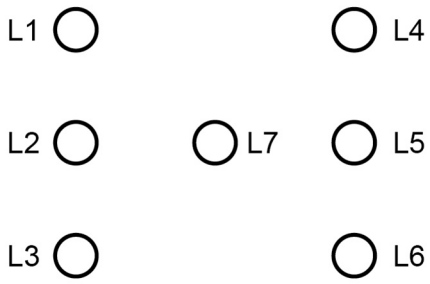
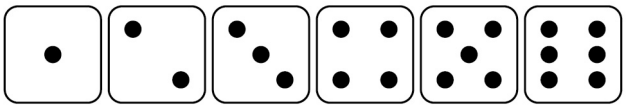


Figure 5 shows the sequence of numbers.

Figure 5



The black dots show which LEDs are lit for each of the numbers 1 to 6.

The partially completed truth table in **Table 1** shows which of the LEDs (L1 to L6) are ON (logic 1) and which are OFF (logic 0) during the counting sequence.

Table 1

Number shown on die	Logic inputs			Logic outputs						
	C	B	A	L1	L2	L3	L4	L5	L6	L7
1	0	0	0		0	0	0	0		1
2	0	0	1		0	0	0	0		0
3	0	1	0		0	0	0	0		1
4	0	1	1		0	1	1	0		0
5	1	0	0		0	1	1	0		1
6	1	0	1		1	1	1	1		0
Reset 6 → 1										

0 1 . 1 Complete **Table 1** to show the logic outputs for the lamps L1 and L6.

[2 marks]

0 1 . 2 Deduce the **simplest** Boolean expression that can be used to show how output L7 can be controlled by the logic inputs.

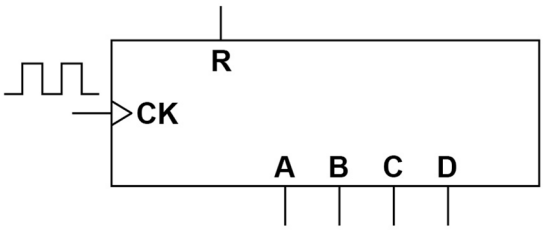
[1 mark]

_____

Turn over ►

0 1 . 3 **Figure 6** shows some of the input and output pins of the 4-bit binary counter.

Figure 6



The data sheet for the counter indicates that the counter resets when the reset pin **R** is taken from logic 0 to logic 1.

Draw on **Figure 6** the logic gate needed and the connections required from the outputs to the reset pin **R** on the counter so that the counter cycles as required.

[2 marks]

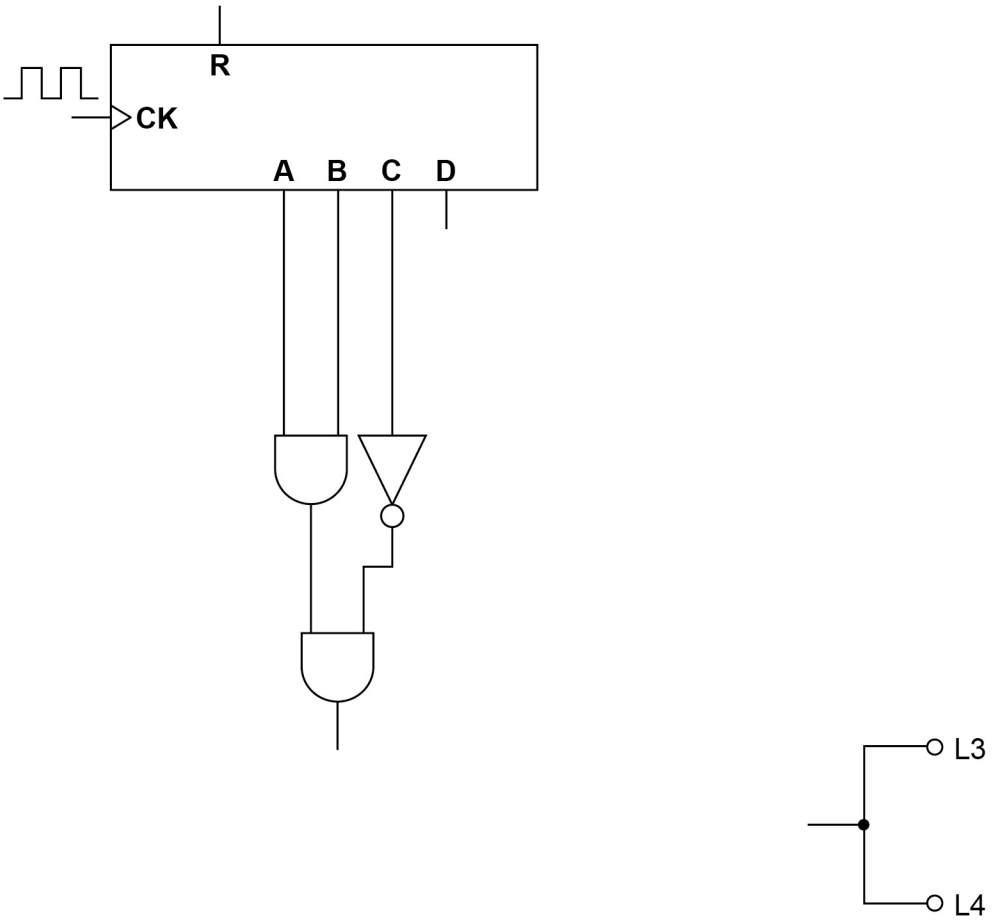
0 1 . 4 The output of both L3 and L4 can be written as **(A . B . $\overline{C}$) + ($\overline{B}$. C)**

Figure 7 shows part of a logic circuit needed to represent this Boolean expression.

Complete the logic circuit in **Figure 7** by adding AND, OR and NOT gates.

[3 marks]

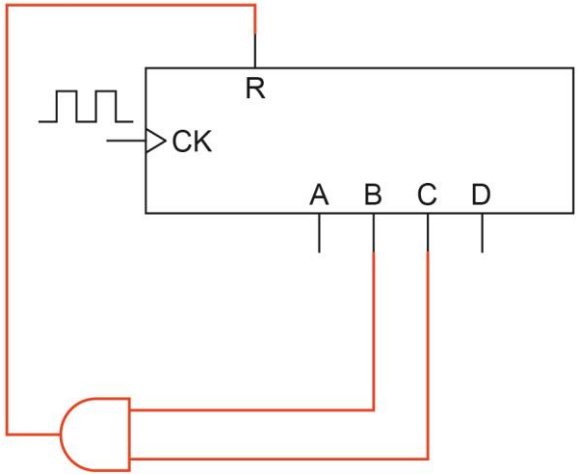
Figure 7

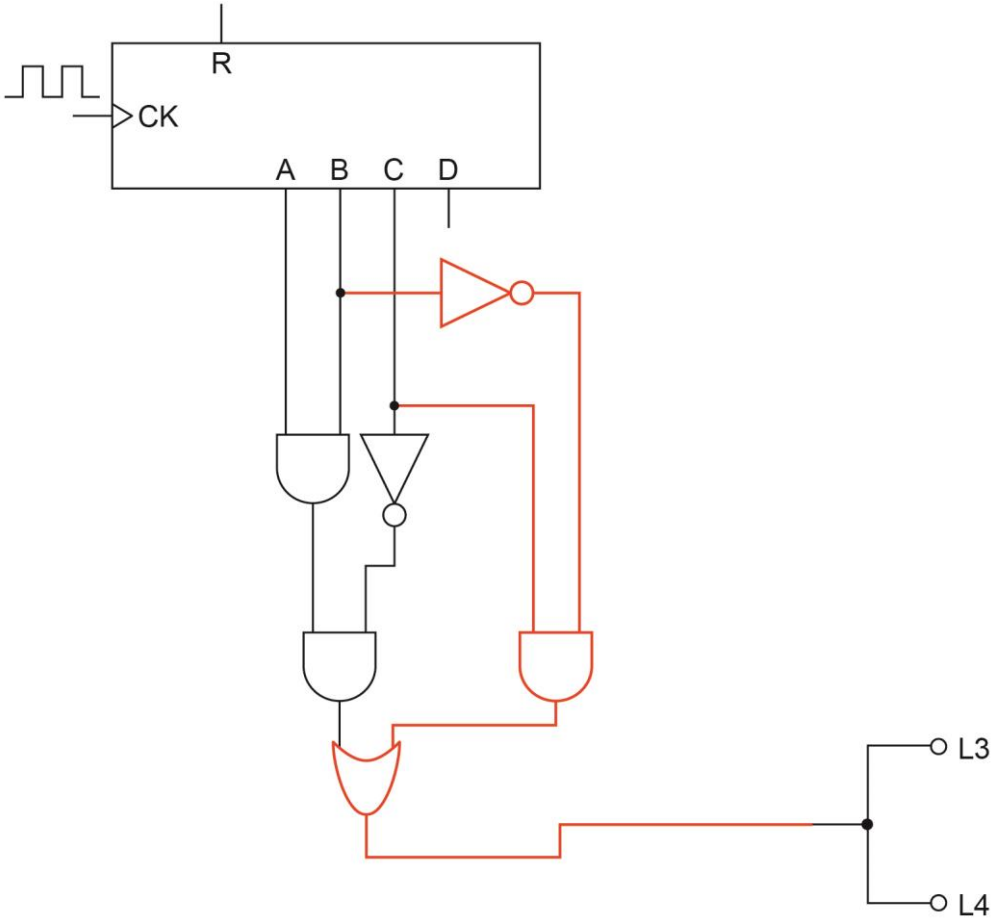


8

Turn over ►

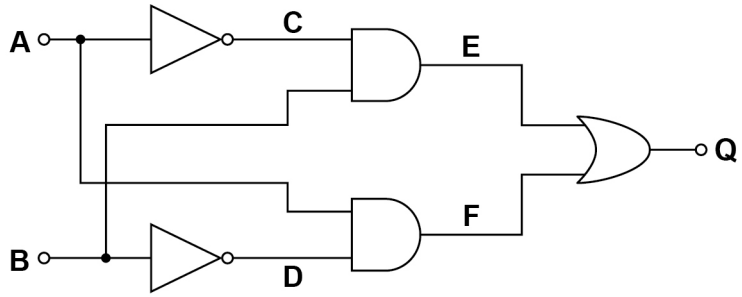
<table>
<tr><th>Question</th><th>Answers</th><th>Additional Comments/Guidelines</th><th>Mark</th></tr>
<tr><td>01.1</td><td>
<table>
<tr><th rowspan="2">Number shown on die</th><th colspan="3">Logic inputs</th><th colspan="7">Logic outputs</th></tr>
<tr><th>C</th><th>B</th><th>A</th><th>L1</th><th>L2</th><th>L3</th><th>L4</th><th>L5</th><th>L6</th><th>L7</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>6</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Reset 6 → 1</td><td colspan="3"></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
</table>
</td><td>One mark for each full pattern of L1 and L6:</td><td>2</td></tr>
<tr><td>01.2</td><td>L7 = NOT A; Accept: L7 = $\bar{A}$</td><td>Delete previous comment</td><td>1</td></tr>
</table>

Question	Answers	Additional Comments/Guidelines	Mark
01.3		1 mark for reset condition from B and C: 1 mark for use of a single 2-input AND gate: (accept correct implementation of the full reset code $\bar{A}$ **.B.C** for 1 mark)	2

Question	Answers	Additional Comments/Guidelines	Mark
01.4		1 mark - NOT gate from B: 1 mark - AND gate from $\bar{B}$ and C: 1 mark - OR gate connecting the two conditions:	3
Total			**8**

0 2 . 1 Two logic inputs, **A** and **B**, feed into the logic circuit shown in **Figure 1**. The logic output from the circuit is **Q**.

Figure 1



Deduce the Boolean expression for the output of this logic circuit in terms of inputs **A** and **B**.
Include all the logic operations that take place between the inputs and the output.

[2 marks]

Q = _____

0 2 . 2 The truth table shows some of the logic states for the logic gates in **Figure 1**.

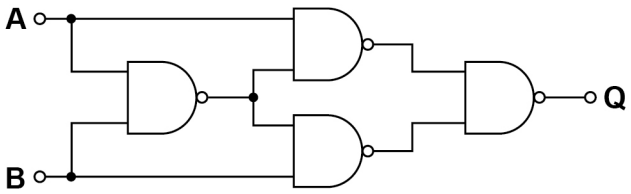
Complete the truth table.

[2 marks]

B	A	C	D	E	F	Q
0	0		1		0	0
0	1		1		1	1
1	0		0		0	1
1	1		0		0	0

0 2 . 3 **Figure 2** shows a different logic circuit that produces the same logic output as that of **Figure 1**.

Figure 2



A manufacturer wants to produce a system that uses this logic function, but is undecided as to which circuit to use.

Suggest, giving reasons, **two** benefits of using the logic circuit in **Figure 2** compared to the logic circuit in **Figure 1**.

[2 marks]

0 2 . 4 State the single logic gate that would perform the same logic function as the circuits shown in **Figure 1** and **Figure 2**.

[1 mark]

7

Turn over ►

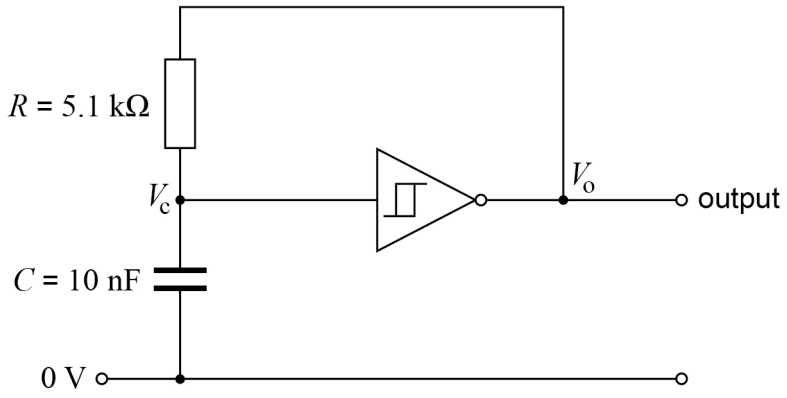
<table>
<tr><th>Question</th><th>Answers</th><th>Additional Comments/Guidance</th><th>Mark</th><th>ID details</th></tr>
<tr><td>02.1</td><td>Q = $(\bar{A}.B) + (A.\bar{B})$ ✓✓ (allow written format)
do not allow (A ⊕ B)</td><td>• Correct two terms ✓
• Correct operator for OR gate ✓</td><td>2</td><td></td></tr>
<tr><td>02.2</td><td><table><tr><th>B</th><th>A</th><th>C</th><th>D</th><th>E</th><th>F</th><th>Q</th></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>✓ ✓</td><td>Correct column C

Correct column E</td><td>2</td><td></td></tr>
<tr><td>03.3</td><td>Any two criteria ✓✓

Less complex circuit – easier to manufacture
Only uses one type of chip – more economical to buy
Uses fewer ICs so saves space
Uses fewer ICs so saves on power consumption</td><td>Accept any other valid reason</td><td>2</td><td></td></tr>
<tr><td>02.4</td><td>EOR ✓</td><td>Also allow EXOR, XOR</td><td>1</td><td></td></tr>
<tr><td>Total</td><td></td><td></td><td>7</td><td></td></tr>
</table>

0 3 . 1 **Figure 6** shows an astable circuit based on a NOT logic gate. The symbol in the centre of the logic gate means that the output V_o changes at two different input values of V_c depending on whether the input voltage is rising or falling.

Figure 6



The pulse repetition frequency (PRF) for this particular circuit is given by:

$$\frac{1}{1.4\,RC}$$

Calculate the PRF in kHz

[1 mark]

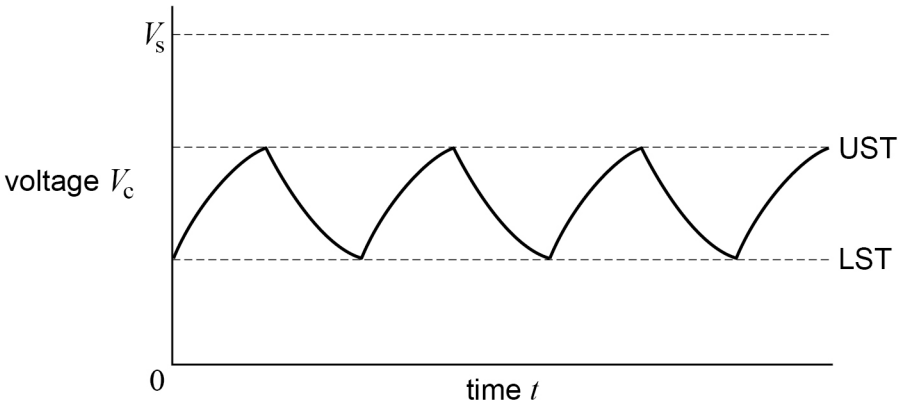
PRF = _____ kHz

0 3 . 2 The supply voltage to the NOT gate is V_s

- When V_c increases and reaches the upper switching threshold (UST), the output of the NOT gate will switch from V_s to 0 V
- When V_c decreases and reaches the lower switching threshold (LST), the output of the NOT gate will switch from 0 V to V_s

The graph in **Figure 7** shows V_c constantly changing as the capacitor charges and discharges.

Figure 7



Draw on **Figure 7** the output voltage V_o for the astable circuit.

[1 mark]

0 3 . 3 The circuit in **Figure 6** can be modified by the addition of a resistor to vary the PRF.

The astable is to be modified so that it produces a frequency 4 times that of the original.

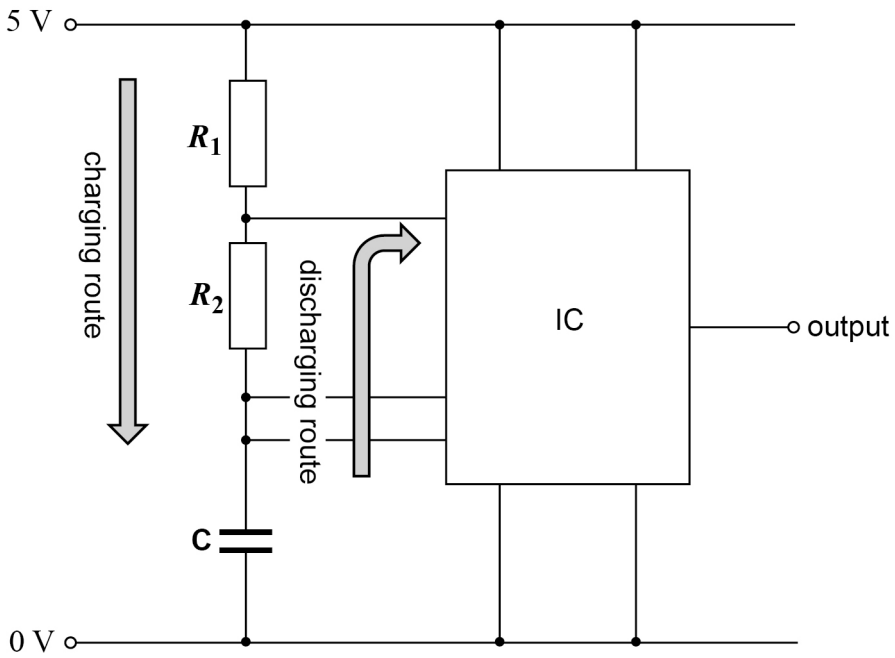
Calculate the value of the resistor that should be added to the circuit and explain where in the circuit this additional resistor should be placed.

[2 marks]

value of resistor = _____ kΩ

0 3 . 4 In another astable, two resistors (R_1 and R_2) and a capacitor **C** form a timing chain to control the mark and space times for a square wave produced at the output of the integrated circuit (IC) shown in **Figure 8**.

Figure 8



The charging time for the capacitor **C** is: $t_C = 0.7 \times (R_1 + R_2) \times C$
The discharging time for the capacitor **C** is: $t_D = 0.7 \times R_2 \times C$

Calculate, in kΩ, values for R_1 and R_2 needed to produce a 5 kHz signal with 75% duty cycle given that the capacitor **C** has a value of 10 nF

[2 marks]

R_1 = _____ kΩ

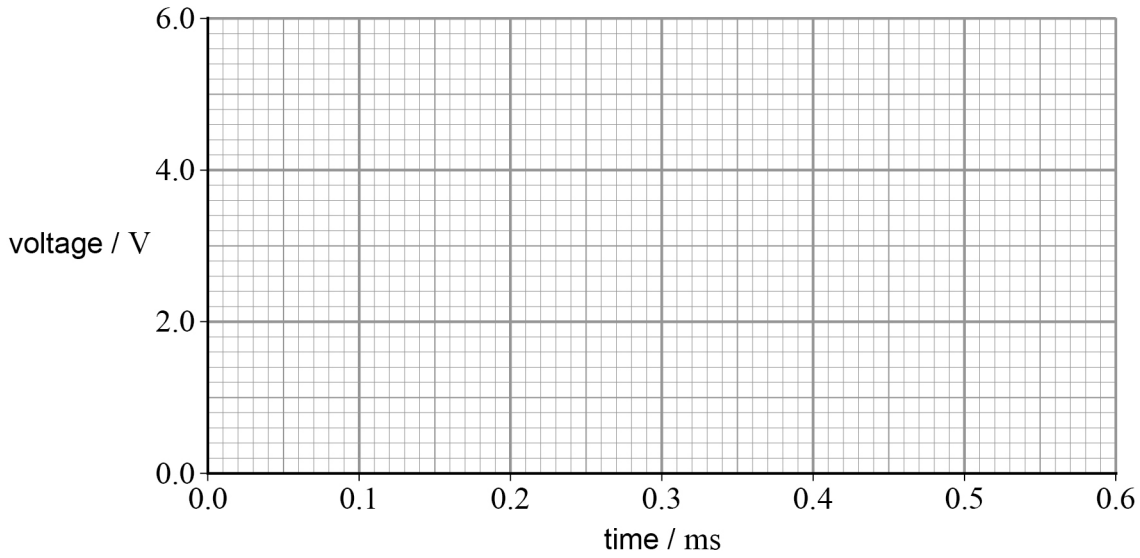
R_2 = _____ kΩ

0 3 . 5 The output of the IC in **Figure 8** is 5 V during the charging period and 0 V during the discharging period.

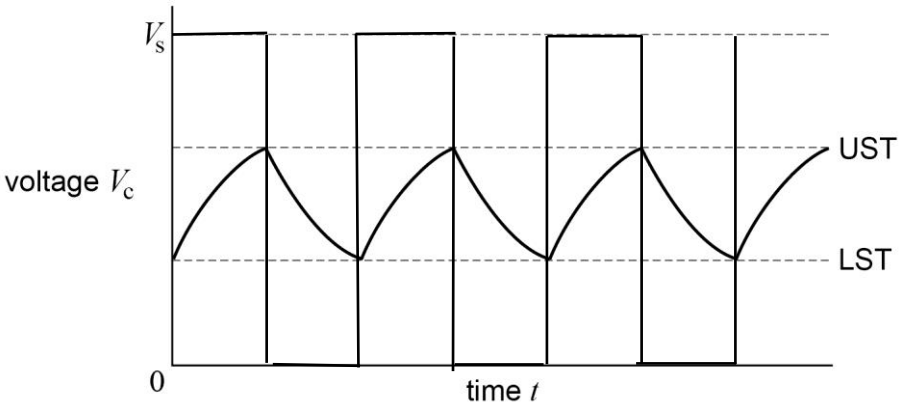
Draw on **Figure 9** the wave pattern that represents this signal.

[2 marks]

Figure 9



8

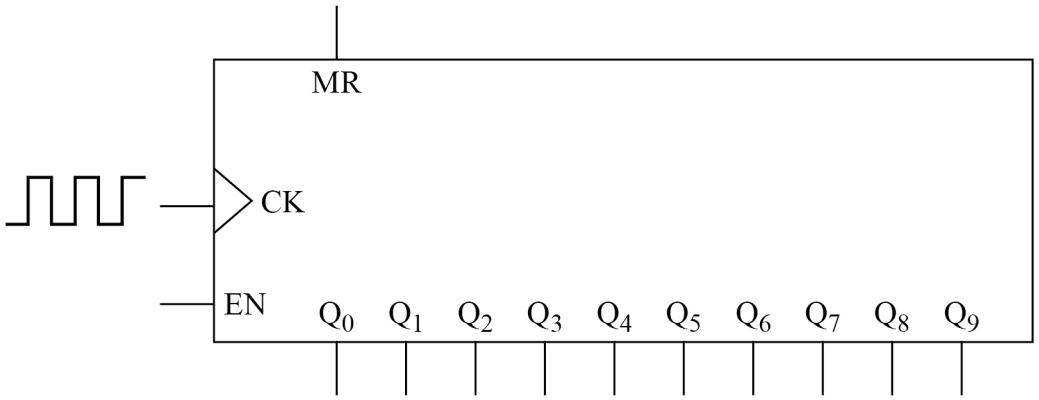
Question	Answers	Additional Comments/Guidance	Mark	ID details
03.1	PRF = $1 / (1.4\ RC)$ = $1 / (1.4 \times 5.1 \times 10^{3} \times 10 \times 10^{-9})$ 14 kHz ✓		1	
03.2	Square wave with correct phase and amplitude ✓ 		1	
03.3	New resistor calculated and stated to be $1.7\ k\Omega$ ✓ New resistor placed in parallel with original resistor ✓	ecf from 04.1	2	

Question	Answers	Additional Comments/Guidance	Mark	ID details
03.4	$T = \frac{1}{f} = \frac{1}{5 \times 10^3} = 0.2$ ms (200 µs) $t_C = 0.2 \times 10^{-3} \times \frac{3}{4} = 150$ µs $t_D = 0.2 \times 10^{-3} \times \frac{1}{4} = 50$ µs $R_2 = \frac{t_D}{0.7 \times C} = \frac{50 \times 10^{-6}}{0.7 \times 10 \times 10^{-9}} = 7.1$ kΩ (Accept 7kΩ) $R_1 = \frac{t_C}{0.7 \times C} - R_2 = 14.3$ kΩ (Accept 14kΩ)	1 mark for significant calculation. eg showing $R_1 = 2R_2$ OR calculation for t_C or t_D 1 mark for values of R_1 and R_2	2	
03.5	Two properties per mark – (max mark 2)✓✓ • A square wave • Amplitude of 0 V to 5 V • Periodic time of 0.2 ms • High for 0.15 ms – Low for 0.05 ms		2	
Total			**8**	

Do not write outside the box

0 4 **Figure 1** shows the basic layout for a Johnson decade counter.
The main input is the clock (CK).
The main outputs are shown as Q_0 to Q_9.

Figure 1

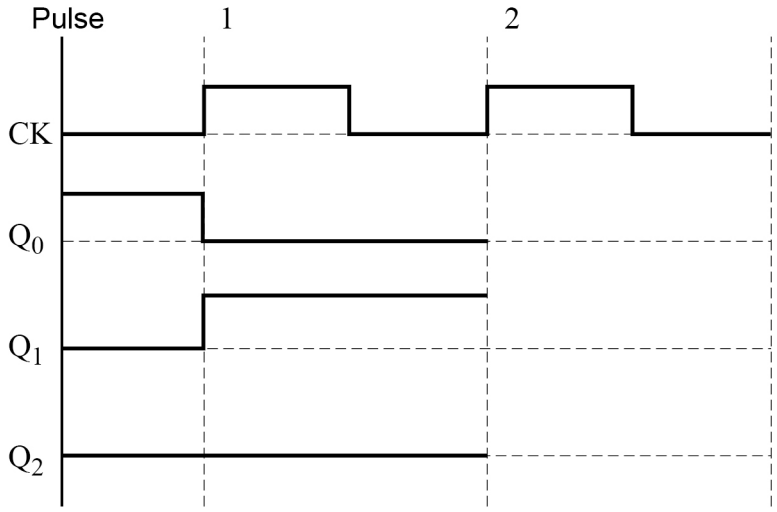


0 4 . 1 **Figure 2** shows part of the timing diagram for a Johnson decade counter.
This timing diagram shows the output logic states against time. The counter is reset to make $Q_0 = 1$ and then the first two pulses are applied.

Complete **Figure 2** to show the logic states of Q_0, Q_1 and Q_2.

[2 marks]

Figure 2



Turn over ►

Do not write outside the box

0 4 . 2 A student sets up the counter to make the traffic light sequence:

red → red + amber → green → amber

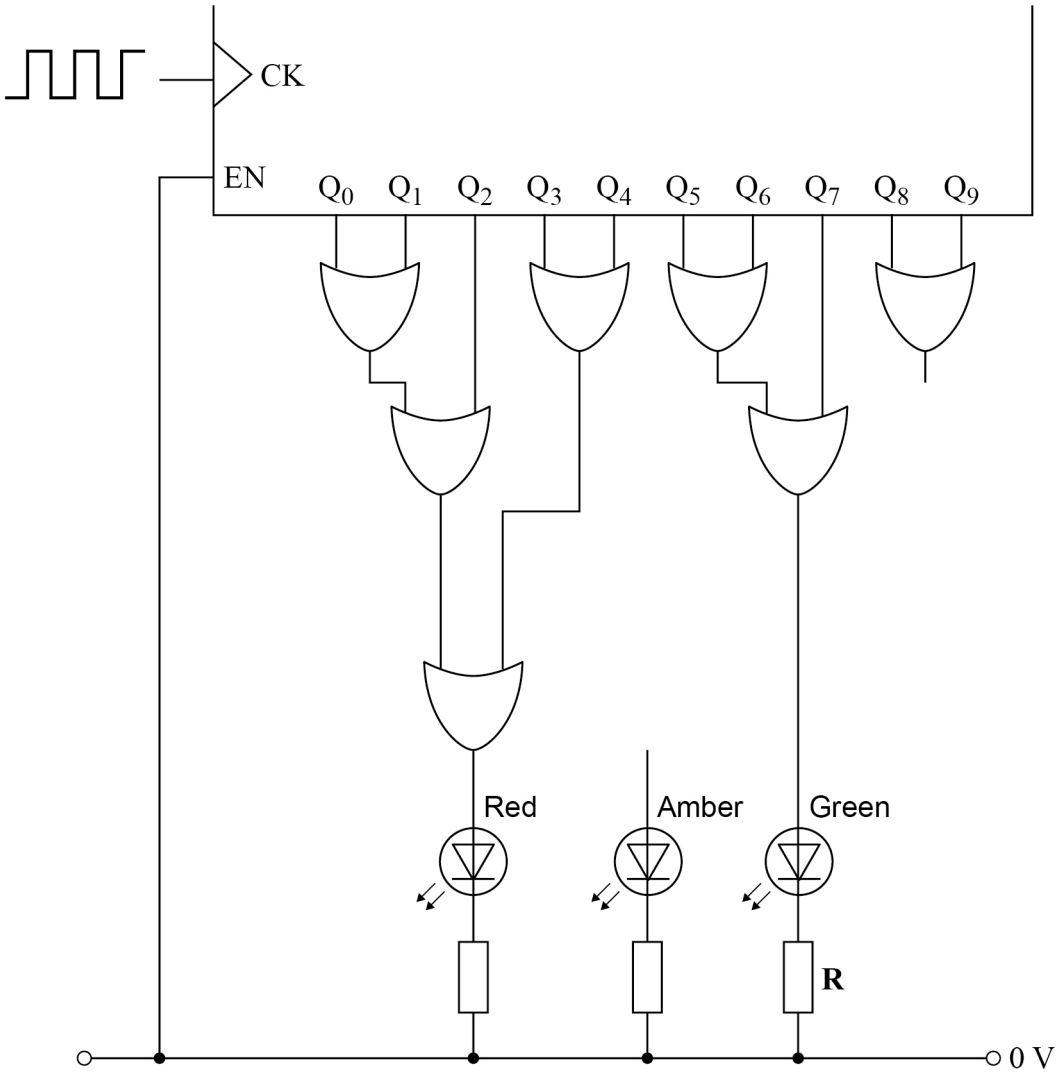
The sequence then repeats.

Figure 3 shows a partially completed diagram for producing this sequence.

Draw an OR gate and connections on **Figure 3** so that the LEDs go through the complete sequence.

[1 mark]

Figure 3



Do not write outside the box

0 4 . 3 State **two** factors that determine the ON time for the green LED shown in **Figure 3**.

[2 marks]

1 _____

_____

2 _____

_____

0 4 . 4 The potential difference across the green LED is $2.1\ \text{V}$ when it is lit. The current through it should not exceed $9\ \text{mA}$.

All logic gate outputs are:
logic low = $0\ \text{V}$
logic high = $9\ \text{V}$.

The student suggests that a resistor of resistance $720\ \Omega$ and a tolerance of $\pm 5\%$ should be used for $\mathbf{R}$.

Deduce whether the student's suggestion would be suitable.

[3 marks]

_____

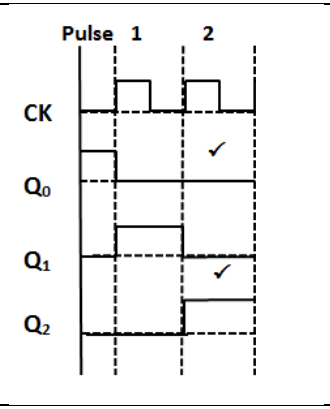
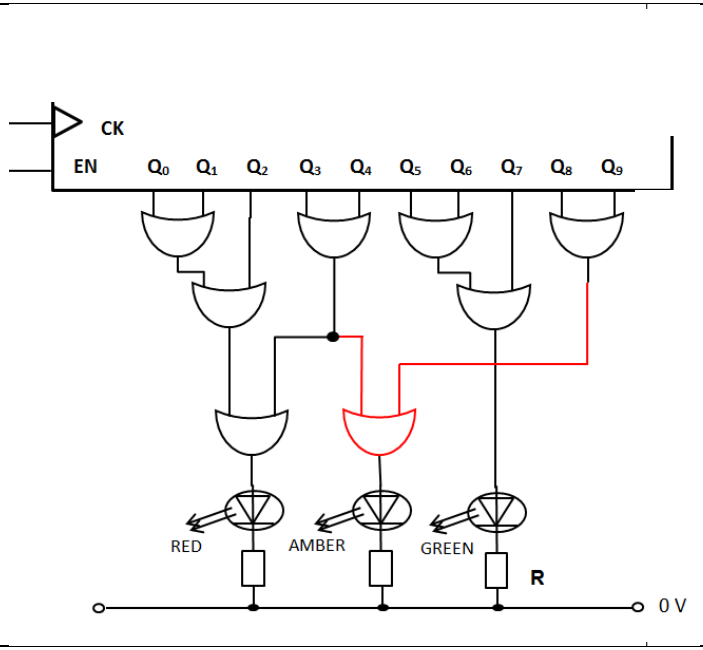
_____

_____

_____

8

Turn over ►

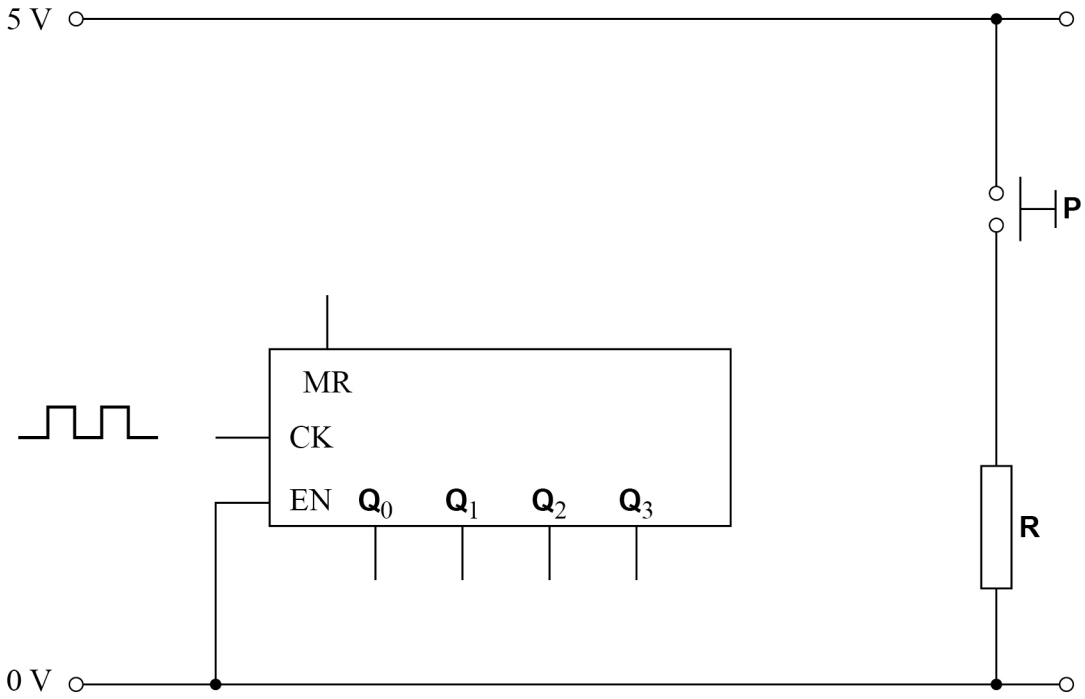
Question	Answers	Additional Comments/Guidance	Mark	ID details
04.1		Flat line of $\mathbf{Q_0}$ - 1 mark Correct fall of $\mathbf{Q_1}$ and rise of $\mathbf{Q_2}$ - 1 mark	2	AO2 1c
04.2		Logic OR gate correctly connected in position for 1 mark	1	AO3 2a

Question	Answers	Additional Comments/Guidance	Mark	ID details
04.3	The ON time for the green LED is determined by: the frequency of the clock ✓ the number of adjacent outputs that are OR'ed ✓	Accept reference to the period of the clock pulse.	2	AO2 1c
04.4	**R** = V_R / I ; **R** = (9 – 2.1) V ✓ / 9 mA **R** = 6.9 V / 9 mA ; **R** = 767 Ω ✓ Minimum resistor value that can be used in order not to exceed 9 mA is 767 Ω. The 720 Ω resistor range is (684 to 756) Ω and falls below this value so should not be used. ✓ OR Calculation using 720 Ω ±5% Resistor range = (684 to 756) Ω ✓ leading to smallest current of 9.1 mA ✓ This current will exceed the permitted value of 9 mA. Don't use. ✓	1One mark for voltage across the resistor 2One mark for a suitable I-V-R calculation 3One mark for conclusion with reason. Use of error range to give max resistance must be seen in either 2 or 3 for that mark to be awarded.	3	AO3 1a AO3 1b
Total			**8**	

Do not write outside the box

0 5 **Figure 1** shows part of a circuit that includes a 4-bit binary counter. The main inputs and outputs of the counter are shown.
The counter generates a sequence of binary codes representing the decimal numbers 0 to 7
Output $\mathbf{Q}_0$ is the least significant bit of the binary codes.

Figure 1



The counter resets when the master reset pin MR receives a logic 1

The circuit requires the counter to reset when either one of two conditions is met.

Condition 1 Manual reset using the switch **P** to reset the counter to 0

Condition 2 Automatic reset when an appropriate binary code is produced at the counter outputs. This will cause the counter to continually cycle through the decimal numbers 0 to 7

0 5 . 1 Complete **Figure 1** to show how both reset conditions can be met.

Do **not** show the power line connections to the integrated circuit.

[3 marks]

Turn over ►

Do not write outside the box

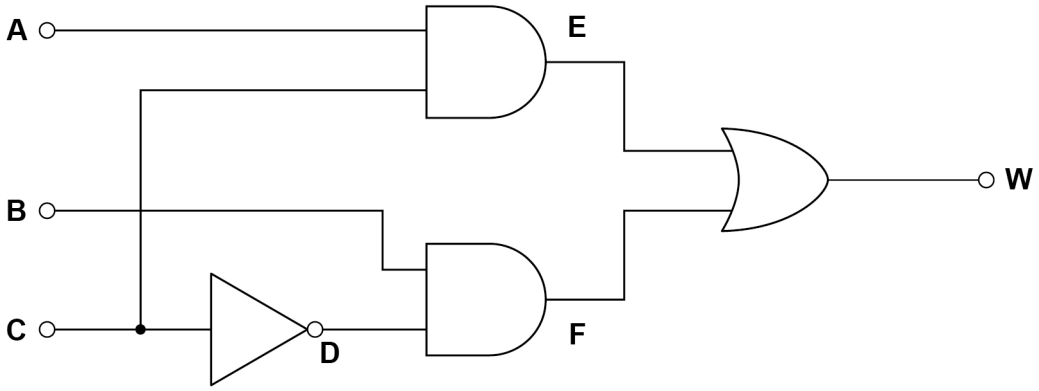
0 5 . 2 A logic system is designed to identify prime numbers.

The binary codes from the counter are now applied to the inputs **ABC** of the logic system shown in **Figure 2**.

Input **A** takes the least significant bit of the binary code from the counter.

Output **W** becomes logic state 1 when a prime number 2, 3, 5 or 7 is detected. Otherwise output **W** is at logic 0

Figure 2



Write the Boolean algebra expression for output **W** in terms of the inputs **A**, **B** and **C**. The expression must contain only the four logic gate operations shown in **Figure 2**.

[2 marks]

W = _____

Do not write outside the box

0 5 . 3 Complete **Table 1**, the truth table for the logic system in **Figure 2**.

[1 mark]

Table 1

Decimal number	C	B	A	D	E	F	W
0	0	0	0	1	0		0
1	0	0	1	1	0		0
2	0	1	0	1	0		1
3	0	1	1	1	0		1
4	1	0	0	0	0		0
5	1	0	1	0	1		1
6	1	1	0	0	0		0
7	1	1	1	0	1		1

0 5 . 4 The logic system in Question **01.2** is replaced with one that gives an output **S** using the same binary input codes **CBA**.

The Boolean algebra equation for output **S** is

$$\mathbf{S} = \overline{\mathbf{A}} . (\mathbf{B} + \mathbf{C})$$

Deduce which decimal numbers 0 to 7 will cause **S** to become logic 1

[1 mark]

Do not write outside the box

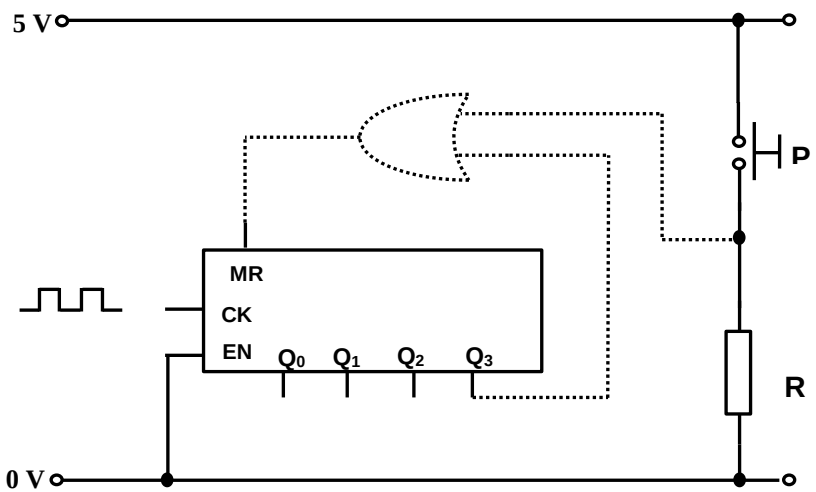
0 5 . 5 Complete **Figure 3** by drawing the logic system for **S**.

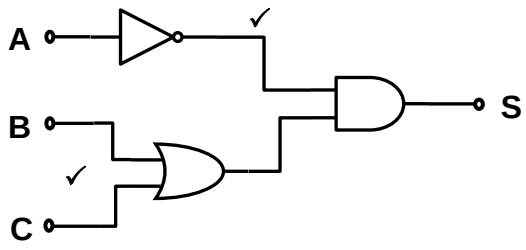
You must use only the logic gate operations given in $\mathbf{S} = \overline{\mathbf{A}} . (\mathbf{B} + \mathbf{C})$

[2 marks]

Figure 3

9

Question	Answers	Additional comments/Guidelines	Mark	AO
05.1	 Correct logic gate to MR ✓ Q_3 to logic gate input ✓ Midpoint of switch chain to logic gate input ✓ OR Accept 2 diodes in correct position ✓✓ Correct orientation ✓	2 marks only for both resets in correct positions but no logic gate. 1 mark only for any correct single reset circuit.	3	AO3.2a AO3.2a AO3.2a
05.2	**(A . C) ✓ + (B . $\overline{C}$) ✓**	Second mark includes the (+)	2	AO2.1h AO2.1h

<table>
<tr><th>Question</th><th>Answers</th><th>Additional comments/Guidelines</th><th>Mark</th><th>AO</th></tr>
<tr><td>05.3</td><td>
<table>
<tr><th>Decimal number</th><th>C</th><th>B</th><th>A</th><th>D</th><th>E</th><th>F</th><th>W</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>3</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>4</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>5</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>6</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>7</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
</table>
</td><td></td><td>1</td><td>AO2.1f</td></tr>
<tr><td>05.4</td><td>numbers 2, 4 and 6 ✓</td><td>accept even numbers</td><td>1</td><td>AO2.1h</td></tr>
<tr><td>05.5</td><td> 
</td><td>NOT A into the AND gate ✓

(B OR C) into the AND gate ✓

Only 1 mark if AND gate is incorrect
.....

Do not accept use of NAND, NOR, EXOR / EXNOR gates to generate equivalent functions.</td><td>2</td><td>AO2.1b
AO2.1b</td></tr>
<tr><td>Total</td><td></td><td></td><td>9</td><td></td></tr>
</table>

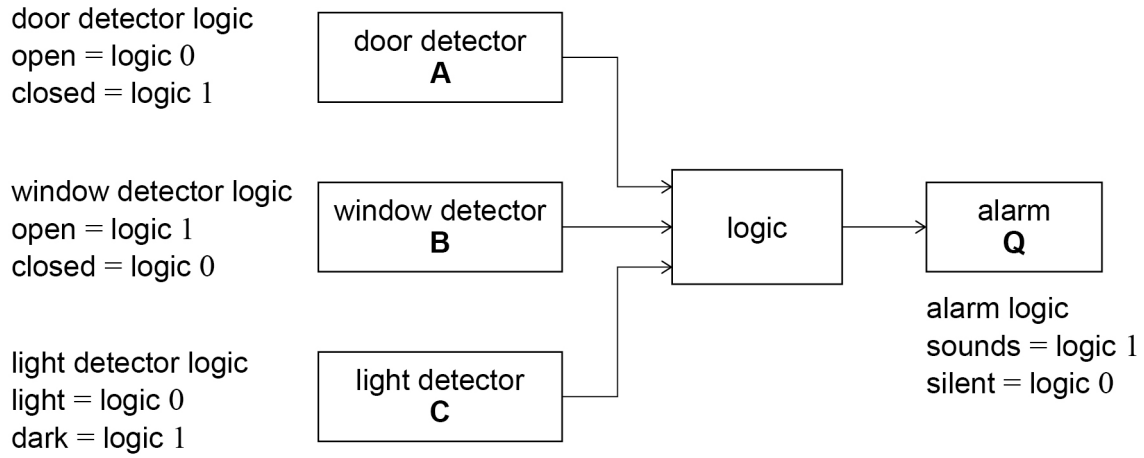
Do not write outside the box

0 6 A burglar-alarm system in a house sounds an alarm during the hours of darkness when **one** of the following conditions is met:

- the door is opened
- the window is opened
- both the door and the window are opened.

Figure 5 shows the main burglar-alarm subsystems and the logic status for the inputs and output.

Figure 5



Do not write outside the box

0 6 . 1 **Table 2** is a partially completed truth table for the logic subsystem.

Table 2

Inputs			Output
C	**B**	**A**	**Q**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	
1	1	0	
1	1	1	

Complete **Table 2**.

[1 mark]

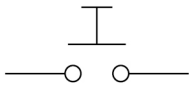
Question 6 continues on the next page

Turn over ►

Do not write outside the box

Figure 6 shows the symbol of the push-to-make switch used in the door detector. When the door is closed, the switch button is pushed down onto the contacts. It automatically releases when the door opens.

Figure 6

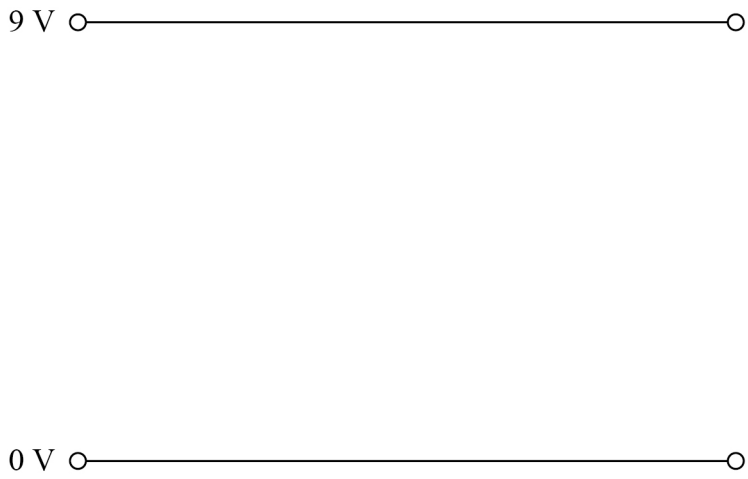


0 6 . 2 Complete **Figure 7** to show how this switch, together with a $10\ \text{k}\Omega$ resistor, can be connected to create the door detector circuit in **Figure 5**.

Label the output of the circuit with an **X**.

[2 marks]

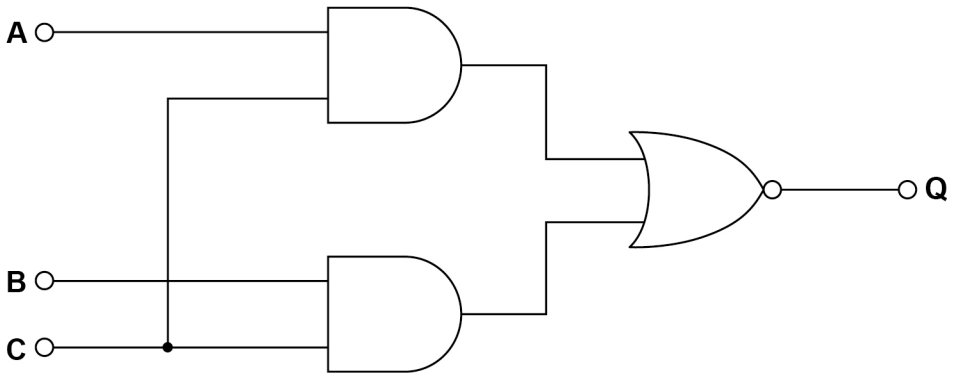
Figure 7



Do not write outside the box

Figure 8 shows a logic circuit for a different alarm system.

Figure 8



0 6 . 3 Write the Boolean algebra expression for **Q** in terms of inputs **A**, **B** and **C**.
In your answer use only AND and NOR operators.

[2 marks]

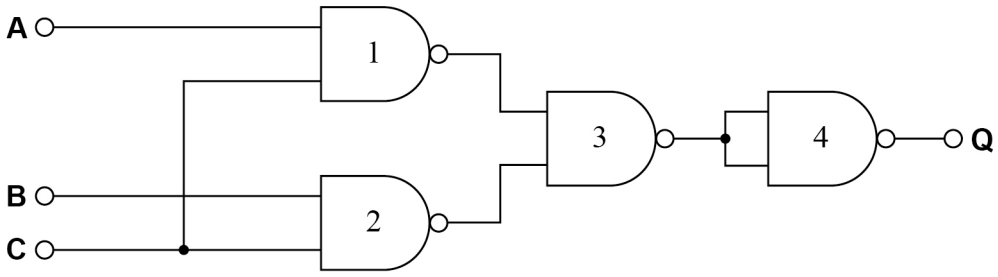
Q = _____

Question 2 continues on the next page

Do not write outside the box

0 6 . 4 **Figure 9** shows a logic circuit that has the same function as the circuit in **Figure 8**. Only one type of gate is used in the circuit in **Figure 9**.

Figure 9



State the logic function performed by gate 4.

[1 mark]

0 6 . 5 Microchips containing two-input logic gates are mass-produced. Each microchip contains four identical logic gates.

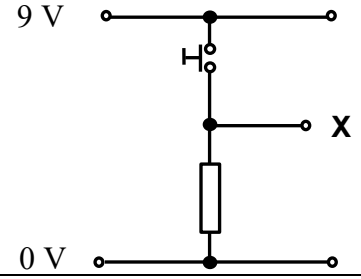
A manufacturer of the logic circuit used in the burglar alarm chooses to make the circuit in **Figure 9** rather than that in **Figure 8**.

Suggest why.

[1 mark]

7

Question	Answers	Additional comments/Guidelines	Mark	AO
06.1	<table><tr><th colspan="3">Inputs</th><th>Output</th></tr><tr><th>C</th><th>B</th><th>A</th><th>Q</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table>	All Q **states** correct for 1 mark	1	AO3 1a

Question	Answers	Additional comments/Guidelines	Mark	AO
06.2		Correct orientation for resistor & switch ✓ Correct tap-off point for **X** ✓	2	AO3 2a AO3 2a

Question	Answers	Additional comments/Guidelines	Mark	AO
06.3	$Q = \overline{(C \,.\, A) + (C \,.\, B)}$ Two correct brackets ✓ + with full bar ✓	Allow for 1 mark: $Q = \overline{C \,.\, (A + B)}$	2	AO2 1b AO2 1b

Question	Answers	Additional comments/Guidelines	Mark	AO
06.4	The gate acts as an inverter ✓	Accept 'NOT' as the function	1	AO1 1a

Question	Answers	Additional comments/Guidelines	Mark	AO
06.5	Must be a reason and a consequence for the mark. ✓	eg Uses only one type of logic gate so need to hold less stock OR Uses only one chip rather than two so circuit board can be smaller / less power needed / cheaper Do not allow: Less complex circuit	1	AO2 1c

Total			7

Do not write outside the box

0 7 A Johnson decade counter uses a Johnson counter together with decoding logic. This arrangement produces a single logic 1 at a series of outputs Q_0–Q_9 in a continuous sequence.

0 7 . 1 Describe **one** functional difference and **one** functional similarity between how a Johnson decade counter and a BCD counter output their counts.

[2 marks]

functional difference _____

_____

_____

_____

functional similarity _____

_____

_____

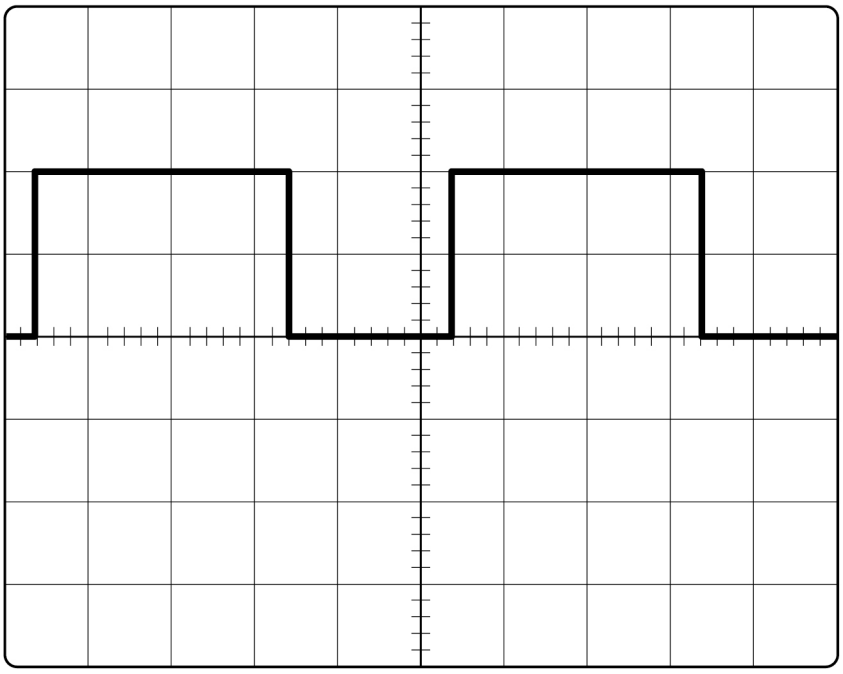
_____

Question 7 continues on the next page

Do not write outside the box

0 7 . 2 An astable oscillator produces a continuous train of pulses.
Figure 13 shows the display of the pulses on an oscilloscope.

Figure 13



The oscilloscope settings are:

voltage gain = 2 V / division
time-base = 50 μs / division.

Determine the duty cycle and frequency of the signal.

[3 marks]

duty cycle = _____

frequency = _____ kHz

Do not write outside the box

0 7 . 3 The astable is adjusted to produce a $600\ \text{Hz}$ test signal.

This signal is applied to the clock input of the BCD counter and to the clock input of the Johnson decade counter.

The outputs of the BCD counter are Q_0, Q_1, Q_2 and Q_3 where Q_0 is the least significant part of the output.
The outputs of the Johnson decade counter are Q_0, Q_1, $Q_2 \ldots Q_9$.

Determine the frequency of the pulses available at Q_2 for each counter.

[2 marks]

BCD counter: frequency of pulses = _____ Hz

Johnson decade counter: frequency of pulses = _____ Hz

7

Turn over ►

Question	Answers	Additional comments/Guidelines	Mark	AO
07.1	**Difference:** BCD counter outputs binary codes. A Johnson decade counter outputs a single output sequentially✓ **Similarity:** Both counters recycle at the 10^{th} pulse ✓	Both outputs described. Condone – max counter value for 10^{th} pulse. Accept: both counters count from 0–9 OR both counters count to 10	2	AO1 1a AO1 1a

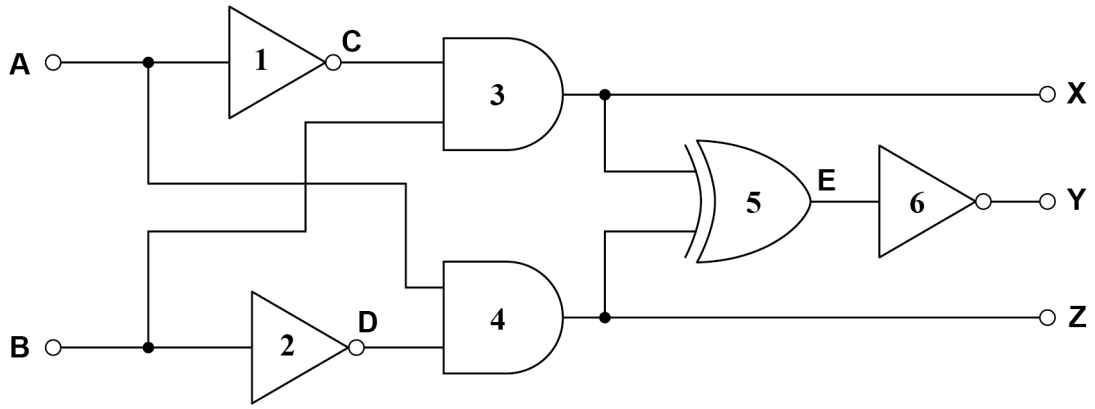
Question	Answers	Additional comments/Guidelines	Mark	AO
07.2	Duty cycle: From oscilloscope $t_{on} = 3$ div @ $50\ \mu s$ / div $= 150\ \mu s$ OR $t_{off} = 2$ div @ $50\ \mu s$ / div $= 100\ \mu s$ ✓ $\frac{t_{on}}{(t_{on} + t_{off})} \times 100 = 60\%$ OR 0.6 ✓ (accept 'divisions' to signify the values of t_{on} and t_{off}) Frequency: From CRO $t_p = 5$ div @ $50\ \mu s$ / div $t_p = 250\ \mu s$ $f = 1/t_p = 4$ kHz ✓	Only 1 mark for: either of t_{on} or t_{off} correct but duty cycle wrong OR correct use of both wrong t_{on} and t_{off} One mark for: correct use of their $t_{on} + t_{off}$	3	AO2 1h AO2 1h AO3 1b

Question	Answers	Additional comments/Guidelines	Mark	AO
07.3	**BCD:** $Q_2 = 600 / 10 = 60$ Hz ✓ (only one pulse is produced in 10 clock pulses at Q_2) **Johnson:** $Q_2 = 600 / 10 = 60$ Hz ✓		2	AO2 1d AO2 1d
Total			**7**	

Do not write outside the box

0 8 **Figure 4** shows a logic system made of logic gates labelled **1** to **6**
The logic system has inputs **A** and **B** and outputs **X**, **Y** and **Z**.

Figure 4



0 8 . 1 Write the simplest Boolean algebra expression for output **X** in terms of inputs **A** and **B**.

[2 marks]

X = _____

0 8 . 2 State the name of logic gate **5** in **Figure 4**.

[1 mark]

_____

0 8 . 3 Complete **Table 1**, the truth table for this logic system.

[2 marks]

Table 1

B	A	C	D	E	X	Y	Z
0	0	1	1	0			
0	1	0	1	1			
1	0	1	0	1			
1	1	0	0	0			

Do not write outside the box

0 8 . 4 Suggest a single logic gate that can replace the combination of gates **5** and **6** in this system.

[1 mark]

0 8 . 5 The logic system in **Figure 4** is designed to indicate which of inputs **A** and **B** has the larger binary value, or whether the values are the same. Each decision is indicated by one of the outputs **X**, **Y** or **Z** becoming a logic 1

Which row identifies the outputs **X**, **Y** and **Z**?
Tick (✓) **one** box.

[1 mark]

X	Y	Z	
A = **B**	**A** < **B**	**A** > **B**	
A < **B**	**A** = **B**	**A** > **B**	
A < **B**	**A** > **B**	**A** = **B**	
A > **B**	**A** = **B**	**A** < **B**	

7

Turn over for the next question

Question	Answers	Additional comments/Guidelines	Mark	AO
08.1	$\overline{A}$ ✓ **.** B ✓ $\overline{\boldsymbol{A}}$ **. B**	Do not allow $\overline{\boldsymbol{A}+\overline{\boldsymbol{B}}}$	2	1 x AO1 1 x AO2

Question	Answers	Additional comments/Guidelines	Mark	AO
08.2	EOR ✓	Accept: XOR ; EXOR; Exclusive OR gate	1	AO1

Question	Answers	Additional comments/Guidelines	Mark	AO
08.3			2	2 x AO2

B	A	C	D	E	X	Y	Z
0	0	1	1	0	**0**	**1**	**0**
0	1	0	1	1	**0**	**0**	**1**
1	0	1	0	1	**1**	**0**	**0**
1	1	0	0	0	**0**	**1**	**0**

X and **Z** correct ✓

Y correct ✓

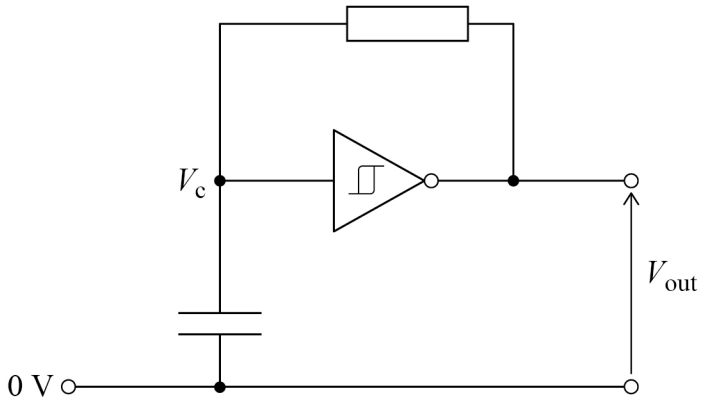
Question	Answers	Additional comments/Guidelines	Mark	AO
08.4	NOR gate ✓	Also accept any of: EXNOR; ENOR; XNOR; Exclusive NOR gate	1	AO3

Question	Answers	Additional comments/Guidelines	Mark	AO
08.5	**X** **Y** **Z** A = B | A < B | A > B | ☐ A < B | A = B | A > B | ✓ A < B | A > B | A = B | ☐ A > B | A = B | A < B | ☐		1	AO2
Total			**7**	

Do not write outside the box

0 9 **Figure 6** shows a type of NOT gate called a Schmitt Trigger. This is connected to a capacitor of capacitance C and a resistor of resistance R to make an oscillator circuit. The circuit is used to produce continuous clock pulses.

Figure 6



V_{out} switches HIGH or LOW when the input voltage V_c passes through one of two trigger voltage values.

The output voltage V_{out} switches to:

- LOW when V_c rises and reaches the upper trigger voltage V_U
- HIGH when V_c falls and reaches the lower trigger voltage V_L.

Do not write outside the box

0 9 . 1 Initially the capacitor is uncharged and V_c is at 0 V.

Explain the sequence of actions of this circuit as the output goes through one full cycle. The first two stages have been done for you.

You should refer to the RC circuit in **Figure 6** and to V_U and V_L in your answer.

[3 marks]

Stage 1: Since V_c is LOW, the output is HIGH.

Stage 2: The capacitor now charges through the resistor, making V_c rise.

Stage 3: _____

_____

_____

Stage 4: _____

_____

_____

Stage 5: _____

_____

_____

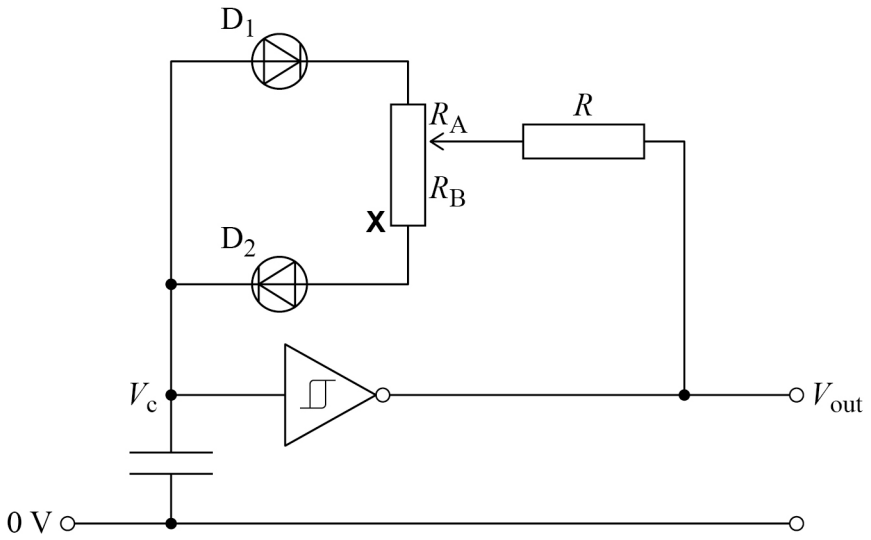
Question 9 continues on the next page

Do not write outside the box

0 9 . 2 **Figure 7** shows the oscillator circuit after it has been modified by the addition of:

- two diodes D_1 and D_2
- a potential divider that has a total resistance value of (R_A + R_B).

Figure 7



In this particular circuit:

- the time t_H for the output signal to be HIGH is given by $t_H = 0.7C\,(R + R_B)$
- the time t_L for the output signal to be LOW is given by $t_L = 0.7C\,(R + R_A)$.

Do not write outside the box

The slider of the potential divider is moved towards **X**, as shown in **Figure 7**.

State and explain the effect of this change on:

- the mark-to-space ratio ($t_H : t_L$)
- the pulse rate frequency (PRF).

[4 marks]

mark-to-space ratio

PRF

7

Question	Answers	Additional comments/Guidelines	Mark	AO
09.1	• When V_c reaches a value of V_U, the output voltage V_{out} drops LOW. ✓ • The capacitor now discharges through the resistor causing the value of V_c to fall. ✓ • When V_c reaches a value of V_L, the output voltage V_{out} jumps HIGH. ✓		3	3 x AO2

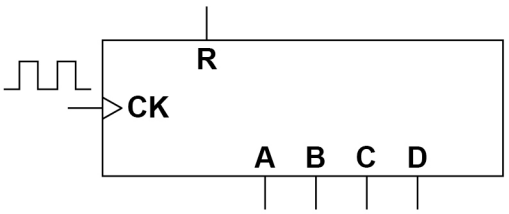
Question	Answers	Additional comments/Guidelines	Mark	AO
09.2	**Mark-to-space ratio** R_B gets smaller and hence (t_H) is reduced OR R_A gets bigger and hence (t_L) is increased ✓ Hence mark:space ratio is reduced / smaller ✓ **PRF** = $\frac{1}{T} = \frac{1}{(t_H + t_L)} = \frac{1}{0.7C\,(2R+R_A+R_B)}$ The total resistance ($2R + R_A + R_B$) is constant ✓ As a result of a constant resistance in the circuit, PRF does not change ✓	First mark: Either statement or equivalent labelled diagram(s). Second mark: Conclusion First mark: explanation of how total resistance in the circuit affects the periodic time. Second mark: Conclusion	4	4 x AO3

Total			7

Do not write outside the box

1 0 **Figure 1** shows the input and output pins for a 4-bit binary counter. The output pin for the least significant bit is **A**.

Figure 1

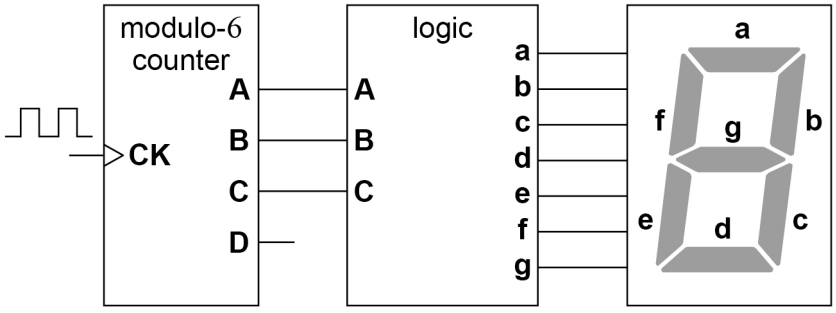


1 0 . 1 Complete **Figure 1** by adding a single logic gate to the binary counter so that the circuit functions as a modulo-6 counter.

[2 marks]

Figure 2 shows three outputs of the modulo-6 counter connected to a logic sub-system that controls a 7-segment display.
The decimal point on the display is not shown.
The whole system shown in **Figure 2** is to be used as an electronic dice.

Figure 2



Segments in the 7-segment display are turned on or off by the logic sub-system to display the decimal numbers 1 to 6 in sequence.
A segment in the display turns on when the logic output with the same letter as the segment is at logic 1.

Do not write outside the box

Table 1 shows how the values of **CBA** control the logic level applied to each of the segments **a** to **g** during the counting cycle.

Table 1

Logic inputs			Logic outputs						
C	**B**	**A**	**a**	**b**	**c**	**d**	**e**	**f**	**g**
0	0	0	0	1	1	0	0	0	0
0	0	1	1	1	0	1	1	0	1
0	1	0	1	1	1	1	0	0	1
0	1	1	0	1	1	0	0	1	1
1	0	0	1	0	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1

1 0 . 2 One of the logic outputs **a** to **g** is controlled by a single NOT gate. This gate uses one of the inputs **A**, **B** or **C**.

State the input that is used and the segment that this NOT gate controls.

[1 mark]

input = _____

segment = _____

1 0 . 3 **X** represents one of the logic outputs. The Boolean expression for this output is:

$$\mathbf{X} = (\mathbf{A} \cdot \mathbf{B}) + \mathbf{C}$$

State which of the logic outputs **a** to **g** is being controlled by this function.

[1 mark]

logic output = _____

Question 10 continues on the next page

Turn over ►

Do not write outside the box

1 0 . 4 **Y** represents another of the logic outputs. The Boolean expression for this output is:

$$Y = \left(\overline{A} \cdot \overline{B}\right) + \left(\overline{\overline{B} \cdot \overline{C}}\right)$$

Complete **Figure 3** to show the combination of logic gates needed to represent the expression.
You should only use logic gates that represent the individual functions shown in the expression.

[3 marks]

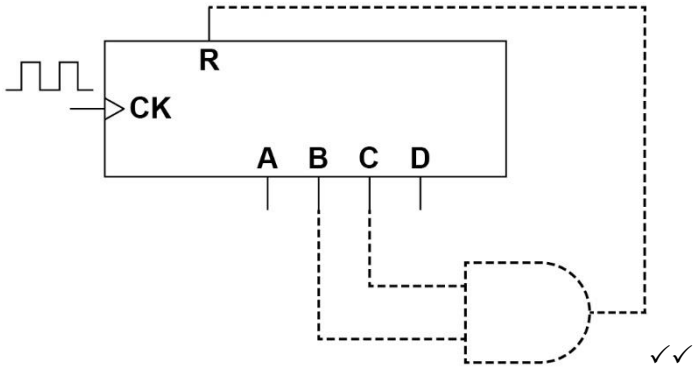
Figure 3

A ○

B ○ ○ **Y**

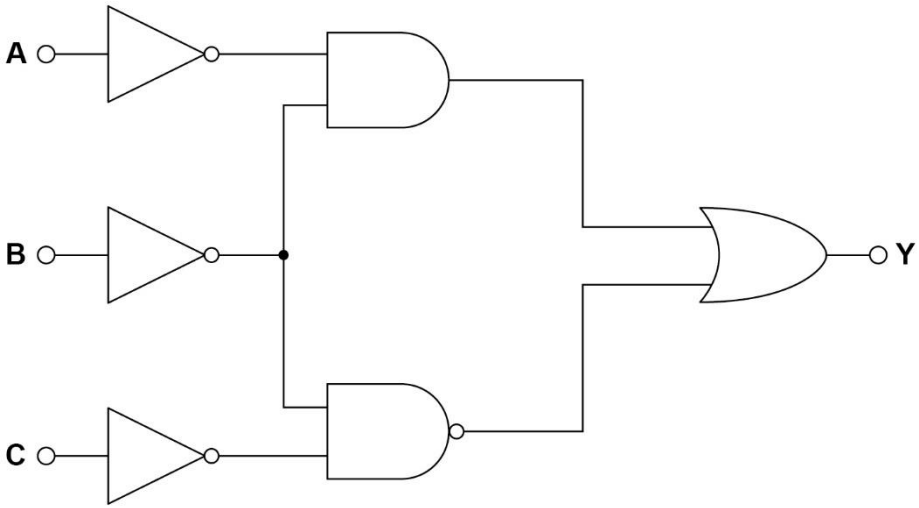
C ○

7

Question	Answers	Additional comments/Guidelines	Mark	AO
10.1	 ✓✓	1 mark for use of the correct counter outputs 1 mark for the correct logic gate connected to reset **R**	2	1× AO2 1 x AO3

Question	Answers	Additional comments/Guidelines	Mark	AO
10.2	input **C** segment **b** ✓	Both input and segment needed for the mark Do not allow **B** for **b**	1	1 × AO2

Question	Answers	Additional comments/Guidelines	Mark	AO
10.3	**f** ✓	Allow **F** for **f**	1	1 × AO3

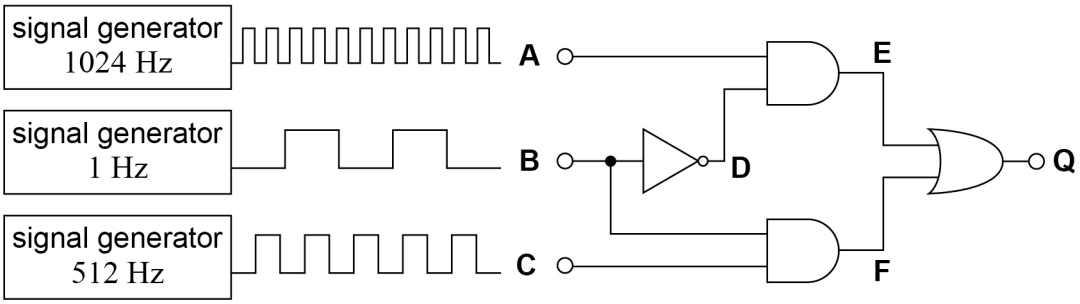
Question	Answers	Additional comments/Guidelines	Mark	AO
10.4	 ✓✓✓	**MP1**: all inputs inverted (accept a shorted-out NAND or NOR gates for the inverters) **MP2:** for correct use of AND and NAND Condone a NOT following an AND for the NAND gate. **MP3:** for final gate being OR	3	3 × AO3
Total			**7**	

Do not write outside the box

1 1 A toy manufacturer is designing a two-tone siren for use in small battery-operated cars.
Figure 1 shows design Option **1**.

Option **1** uses three separate signal generators feeding into a logic sub-system.
The signal generators produce logic-compatible 9 V square waves of frequencies 1024 Hz, 1 Hz and 512 Hz.

Figure 1



The waveforms shown are not to scale.

1 1 . 1 Explain how the logic level applied at **B** in **Figure 1** determines the output frequency at **Q**.

[2 marks]

1 1 . 2 Write the Boolean algebra expression for output **Q** in terms of the inputs **A**, **B** and **C**.
Use only the logic operations shown in **Figure 1**.

[2 marks]

Q = _____

Do not write outside the box

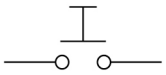
1 1 . 3 Option **1** is tested by replacing the $1\ \text{Hz}$ signal generator with a manual input.

The manual input is provided by the combination of a push-to-make switch and a $10\ \text{k}\Omega$ resistor.

The combination produces the following voltages at its output:
- $0\ \text{V}$ when the switch is not pressed
- $9\ \text{V}$ when the switch is pressed.

Figure 2 shows the symbol for the push-to-make switch.

Figure 2



Complete **Figure 3** to show how this switch and the $10\ \text{k}\Omega$ resistor are connected.
Label the output V_{out}.
You do not need to add details taken from **Figure 1**.

[1 mark]

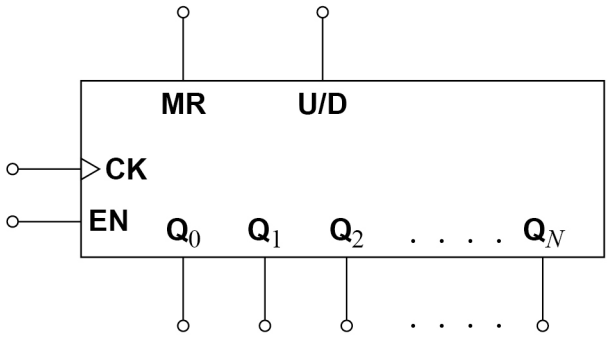
Figure 3

Question 11 continues on the next page

Do not write outside the box

1 1 . 4 **Figure 4** shows a generalised layout of an integrated circuit (IC) for an N-bit binary counter.
$\mathbf{Q}_0$ is the output that provides the least significant bit.

Figure 4



A signal generator feeds a square wave of frequency 1024 Hz into the clock of the IC. The N-bit binary counter generates the 512 Hz signal and the 1 Hz signal from separate outputs.

Deduce which of the outputs $\mathbf{Q}_0$ to $\mathbf{Q}_N$ will provide the 1 Hz signal.

[1 mark]

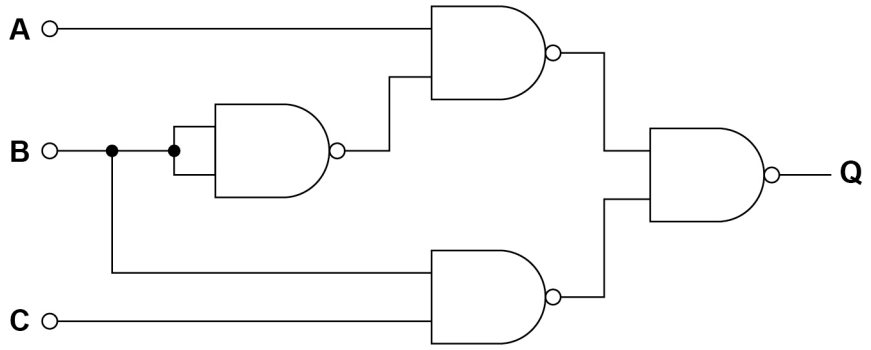
Do not write outside the box

1 1 . 5 To make the two-tone siren, the manufacturer decides to use a new design, Option **2**.

Option **2** contains:

- one 1024 Hz signal generator
- one N-bit binary counter
- a new logic sub-system as shown in **Figure 5**.

Figure 5



Assume that:

- each **type** of logic gate has its own dedicated IC chip
- each separate signal generator is based upon its own IC chip.

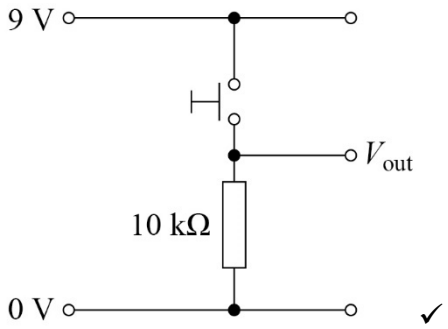
Compare the number of ICs used in Option **1** with the number used in Option **2**.
Go on to explain **one** advantage of the manufacturer's decision.

[2 marks]

8

Question	Answers	Additional comments/Guidelines	Mark	AO
11.1	When B = logic 0, (point D is logic 1.) (Result: closes the lower AND gate and opens the upper AND gate.) Only the $1024\ \text{Hz}$ signal is allowed to (pass through to the OR gate) output Q. ✓ When B = logic 1,(point D is logic 0). (Result: closes the upper AND gate and opens the lower AND gate.) Only the $512\ \text{Hz}$ signal is allowed to (pass through to the OR gate) output Q. ✓	1st mark: • explanation for either logic 1 or logic 0 input • reference as to which frequency passes through OR gate. 2nd mark: reference to other half of the cycle and output frequency. 1 Max if there is no reference to the action of at least 1 gate.	2	AO2

Question	Answers	Additional comments/Guidelines	Mark	AO
11.2	**Q** = $(A \cdot \overline{B}) + (B \cdot C)$ ✓ ✓	1st mark for: contents of either bracket 2nd mark for: contents of other bracket and the '+'	2	AO2

Question	Answers	Additional comments/Guidelines	Mark	AO
11.3	 ✓	Mark awarded if all the following are present: • resistor and push-to-make switch are in correct position • output point in correct position and labelled.	1	AO3

Question	Answers	Additional comments/Guidelines	Mark	AO
11.4	**Q_9** ✓	$2^{(n+1)} = 1024$ Condone n = 9	1	AO2

Question	Answers	Additional comments/Guidelines	Mark	AO
11.5	Option 1 requires a total of 6 ICs whereas Option 2 requires a total of 3 ICs ✓ Advantage: One from: ✓ • smaller circuit to fit toys • less power consumed / extended battery life • less complex circuits / lower production costs	1st mark: identifies the main advantage (must be numerical) 2nd mark: gives one advantage from the list /or other valid explanation Allow one mark for answers that only consider number of **logic gates** in the two systems leading to the correct conclusion.	2	AO3
Total			**8**	

1 2 The Boolean equation for a particular logic circuit with inputs A and B and output Q is:

$$\mathbf{Q} = (\mathbf{A}.\mathbf{B}) + (\overline{\mathbf{A}}.\overline{\mathbf{B}})$$

1 2 . 1 **Table 1** shows intermediate logic signals for the circuit, and the overall output, Q, for all combinations of the inputs A and B.

Complete the missing two entries in the truth table.

[1 mark]

Table 1

A	B	$\overline{A}$	$\overline{B}$	A . B	$\overline{A}$. $\overline{B}$	Q
0	0	1	1	0	1	
0	1	1	0	0	0	0
1	0	0	1	0		0
1	1	0	0	1	0	1

1 2 . 2 Complete the diagram in **Figure 6** to show the logic circuit that has the same function as the Boolean equation given in part 6**.** Your circuit should contain only **two** AND gates, **two** NOT gates, and **one** OR gate.

[3 marks]

Figure 6

END OF QUESTIONS

12.1			1

A	**B**	$\overline{\mathbf{A}}$	$\overline{\mathbf{B}}$	**A . B**	$\overline{\mathbf{A}} . \overline{\mathbf{B}}$	**Q**
0	0	1	1	0	1	1
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	1	0	0	1	0	1

Both correct

First line Q = 1

Third line Q = 0